Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

Claim 1 (previously presented): A chip scale integrated circuit chip package comprising a die mounted by flip chip interconnection to a first surface of a package substrate, wherein the flip chip interconnection comprises solid state connections of interconnect bumps affixed to the die with interconnect pads on the first surface of the substrate; and second level interconnections formed on the first surface of the package substrate.

Claim 2 (previously presented): The package of claim 1 wherein the die is provided with interconnection bumps affixed to an arrangement of connection sites in a first surface of the die, and the flip chip interconnection comprises solid state connection of the interconnection bumps with a complementary arrangement of interconnect pads on the first surface of the substrate.

Claim 3 (original): The package of claim 1 wherein a gap between the first surface of the die and the first surface of the substrate is at least partly filled with a die attach material.

Claim 4 (original): The package of claim 1 wherein the height of the second level interconnections defines a standoff, and the sum of a thickness of the first die and a gap between the first surface of the die and the first surface of the substrate is less than the standoff.

Claim 5 (canceled)

Claim 6 (original): The package of claim 1 wherein the first die is attached at about the center of the first surface of the substrate, and the solder balls for the second level interconnections are located nearer the periphery of the substrate.

Claim 7 (original): The package of claim 1 wherein a ground plane is optionally provided on the second surface of the substrate.

Claim 8 (original): The package of claim 1 wherein at least some electrical traces are constructed as coplanar waveguides.

Claim 9 (original): The package of claim 1, further comprising a second die attached to a second surface of the substrate.

Claim 10 (original): The package of claim 9 wherein the second die is interconnected to the substrate by wire bonding.

Claim 11 (original): The package of claim 9 wherein the second die is interconnected to the substrate by a flip-chip interconnect.

Claim 12 (new): The package of claim 2 wherein a gap between the first surface of the die and the first surface of the substrate is less than about 0.025 mm.

Claim 13 (new): The package of claim 1 wherein a height of the secondary interconnect solder balls from the first surface of the substrate is about 0.3 mm.

Claim 14 (new): The package of claim 1 wherein an overall package height is about 0.4 mm.

Claim 15 (new): The package of claim 1 wherein an overall package height is less than about 0.4 mm.

Claim 16 (new): The package of claim 1 wherein interconnect geometries in the solid state flip chip connections are in a range less than about 0.1 mm pitch.

Claim 17 (new): The package of claim 6 wherein the solder balls for the second level interconnection are at a pitch about 0.5 mm.